IN THE DRAWINGS

Corrected drawings are supplied herewith.

Enclosed is a Replacement Sheet showing the following amendment to Figures 1 and 2.

Enclosed is a copy of Figure 1 of the drawings showing the following proposed amendment to Figure 1 in red ink. The DATA signals are numbered 0, and 1 through N.

Enclosed is a copy of Figure 2 of the drawings showing the following proposed amendment to Figure 2 in red ink. The DATA signals are numbered 0 through N.

REMARKS

This responds to the Office Action mailed on January 3, 2005, and the references cited therewith.

Claims 1, 3, 17, 19, 20, and 31 are amended, claims 1-40 are pending in this application.

§112 Rejection of the Claims

Claims 1-40 were rejected under 35 U.S.C. § 112, first paragraph, as lacking adequate description or enablement; namely that the specification, while being enabling for "*a first control signal*" and "*a second control signal*", does not reasonably provide enablement for the above limitations.

Applicant respectfully submits that the first and second control signals are enabled by the specification. The Office Action states that the specification does not disclose how to achieve a first or second control signal from one of a predetermined amount of incremented (decremented) high signals. However, the control signals are not derived based on the signals but rather from data (FIG. 2). A plurality of variable incremented high logic signals is output in accordance with the control signals. Page 8 lines 22-23 of the specification state that each of the memory elements (of FIG. 2) has an input to receive the first control signal. Page 11 line 6 states that the input of the memory element 262 (of FIG. 2) receives the second control signal. FIG. 2 shows that the first and second control signals correspond to the DATA signals input to the memory elements.

The Office Action states that the programmable logic circuits are shown to be dependent on a single input, namely DATA (Office Action page 3). FIGS. 1 and 2 are amended to clarify that DATA does not correspond to one single input. If DATA was one single input, the only settings for the flip-flop circuits would be all ones or all zeros, and the adjust circuits would not increment or decrement the separations between edges of the clock signal (page 2 lines 18-20). Because DATA does not correspond to a single input, the Figures and specification enable "inputting first and second programming instructions" recited in claim 39. Applicant respectfully submits that claims 1-40 are enabled by the specification and drawings.

Claims 1-38 were rejected under 35 U.S.C. § 112, second paragraph, for indefiniteness. Claims 1, 3, 17, 19, 20, and 31 were amended to cure the indefiniteness. The specification states that the "incremental and decremental high logic signals" are provided by the first programmable logic circuit (page 8 lines 19-21, and page 8 line 29 through page 9 line 2), that the "incremented and decremented high logic signals" are provided by the second programmable logic circuit (page 11 lines 3-10), and that the "incremented and decremented duty cycle adjusted clock signals are provided by the positive and negative variable duty cycle adjust circuits (page 8 lines 6-9).

Because claims 1-40 are enabled by the specification and drawings in accordance with 35 U.S.C. § 112 first paragraph, and because Applicant believes that claims 1-38 in their present form are not indefinite under 35 U.S.C. § 112 second paragraph, Applicant respectfully requests reconsideration and allowance of claims 1-40.

§102 Rejection of the Claims

Claims 1, 17, 31-34 and 38-39 were rejected under 35 U.S.C. § 102(e) for anticipation by Kwak (US 6,677,792). Applicant respectfully traverses the rejection. To anticipate a claim, the reference must teach every element of the claims. *M.P.E.P. § 2131.*

Regarding claim 1:

Applicant cannot find in Kwak, among other things,

> an output module to receive the incremented and decremented high logic signals and the incremented and decremented duty cycle adjusted clock signals, and to couple to an output clock terminal (CLK OUT) to output an adjusted clock signal having an incremented or decremented duty cycle clock signal as a function of the second control signal,

as presently recited in claim 1. The Office Action apparently states that the blend circuit 130 of Kwak reads on the output module. However, the blend circuit does not include every characteristic of the output module recited in claim 1.

Regarding claim 17:

Applicant cannot find in Kwak,

> an output module to receive the incremented and decremented high logic signals and the incremented and decremented duty cycle adjusted clock signals, and to

> couple to an output clock terminal (CLK OUT) to output the incremented duty cycle adjusted clock signal or the decremented duty cycle adjusted clock signal as a function of the incremented high logic signal or the decremented high logic signal, respectively,

as presently recited in claim 17.

Regarding claims 31-34 and 38:

> Applicant cannot find in Kwak,
>
> inputting a first programmed instruction for selecting one of a plurality of incremented or decremented separations between a raising edge and a falling edge of a clock signal into the integrated circuit device, (and)
> inputting a second programmed instruction for selecting to output the generated one of the plurality of incremented or decremented duty cycle adjusted clock signals,

as recited or incorporated in the claims.

Regarding claim 39:

> Applicant cannot find in Kwak, a method comprising
>
> inputting first and second programming instructions into one of a plurality of edge-triggered circuits to select one of a series of plurality of incremental or decremental duty cycle adjust circuits to adjust the duty cycle of a clock signal as a function of the first and second programming instructions,

as recited in claim 39.

Applicant respectfully requests reconsideration and allowance of claims 1, 17, 31-34 and 38-39.

§103 Rejection of the Claims

Claims 2, 18, 37-38 and 40 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kwak (US 6,677,792) in view of Martin (US 6,040,726). Applicant respectfully traverses the rejection. To establish a prima facie case of obviousness, among other things, the reference must teach or suggest all the claim limitations. *M.P.E.P. § 2143.01*. Claims in dependent form shall be construed to include all the claim limitations incorporated by reference into the dependent claim. *37 C.F.R. § 1.75*.

Claim 2 depends on base claim 1, claim 18 depends on base claim 17, claims 37 and 38 ultimately depend on base claim 31, and claim 40 depends on base claim 39. As discussed previously, Kwak fails to teach or suggest all the elements of base claims 1, 17, 31, or 39 which are incorporated into their dependent claims. The addition of Martin fails to teach or suggest the missing elements.

Applicant respectfully requests reconsideration and allowance of claims 2, 18, 37-38 and 40 at least for the reason that the proposed combination of Kwak and Martin fails to teach or suggest all the claim elements incorporated into the contested claims.

Claims 35 and 36 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kwak (US 6,677,792) in view of Wu et al. (US 6,100,736). Applicant respectfully traverses the rejection.

Claims 37 and 38 ultimately depend on base claim 31. As discussed previously, Kwak fails to teach or suggest all the elements of base claim 31 which are incorporated into dependent claims 37 and 38. The addition of Wu fails to teach or suggest the missing elements. Wu refers to shift registers in Figures 3 and 5B and in Column 4 and refers to shifting data using PREV and NEXT signals (column 4 lines 29-41). Therefore, the combination of Kwak and Wu fails to teach or suggest, among other things, inputting first and second instructions to provide the functionality incorporated into the contested claims.

Applicant respectfully requests reconsideration and allowance of claims 35 and 36.

Allowable Subject Matter

Claims 3-16 and 19-30 were indicated to be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. § 112, 2nd paragraph, set forth in the Office Action and to include all of the limitations of the base claim and any intervening claims.

Applicant acknowledges the allowable subject matter. Claims 3-16 and 19-30 ultimately depend on base claims 1 and 17. Applicant believes the base claims are allowable in their present form at least for the reasons discussed previously.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6909 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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By his Representatives,

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Date July 5, 2005 By Thomas F. Brennan

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 5 day of July, 2005. (Tuesday)

CANDIS BUENDING

Name

Signature